San Diego State University

CS 370 Computer Architecture

Homework Assignment #3

- Please type the solutions using a word processor such as WORD, Latex, etc., or write by hand very neatly and legibly, comparable to typing*.
- Please pay special attention to the due date – no late turn ins or special case consideration.
- Please do not email your homework. Instead, please turn in a paper version of your homework in the classroom. Neither the instructor nor the grader will print your homework for you.
- Please do the following problems from the textbook, and submit solutions:
  1. Problem 6-8
  2. Problem 6-12
  3. Problem 7-3
  4. Problem 7-9
  5. Problem 8-5

* The preferred format is typing with a word processor for the following reasons:
  1. You have a copy in your computer that you can study for exams or future use.
  2. You will learn to use a word processor (if not already learned) to do math, diagrams, etc. This will be one of the most useful things in your career.
  3. You have a backup copy in case of lost or misplaced assignment.
  4. A typed assignment helps the grader to spend less time and to be more accurate in grading. Our class is multi-national, and it is hard and time consuming to decode many different hand writing styles.
6-8. How many flip-flop values are complemented in an 8-bit binary ripple counter to reach the next count value after:

(a) 11111111?          (b) 01100111?          (c) 01010110

6-12. (a) Using the synchronous binary counter of Figure 6-14 and an AND gate, construct a counter that counts from 0000 through 1010.
(b) Repeat for a count from 0000 to 1110. Minimize the number of inputs to the AND gate.

![Figure 6-14: 4-Bit Binary Counter with Parallel Load]

7-3. *A 64K × 16 RAM chip uses coincident decoding by splitting the internal decoder into row select and column select. (a) Assuming that the RAM cell array is square, what is the size of each decoder, and how many AND gates are required for decoding an address? (b) Determine the row and column selection lines that are enabled when the input address is the binary equivalent of (32000)$_{10}$.

7-9. Using the 64K × 8 RAM chip in Figure 7-9 plus a decoder, construct the block diagram for a 1M × 32 RAM.

![Figure 7-9: Symbol for a 64K × 8 RAM Chip]

8-5. Inputs $X_i$ and $Y_i$ of each full adder in an arithmetic circuit have digital logic specified by the Boolean functions

$$X_i = A_i \quad Y_i = \overline{B_i}S + B_i\overline{C_{in}}$$

where $S$ is a selection variable, $C_{in}$ is the input carry, and $A_i$ and $B_i$ are input data for stage $i$.

(a) Draw the logic diagram for the 4-bit circuit, using full adders and multiplexers.

(b) Determine the arithmetic operation performed for each of the four combinations of $S$ and $C_{in}$: 00, 01, 10, and 11.