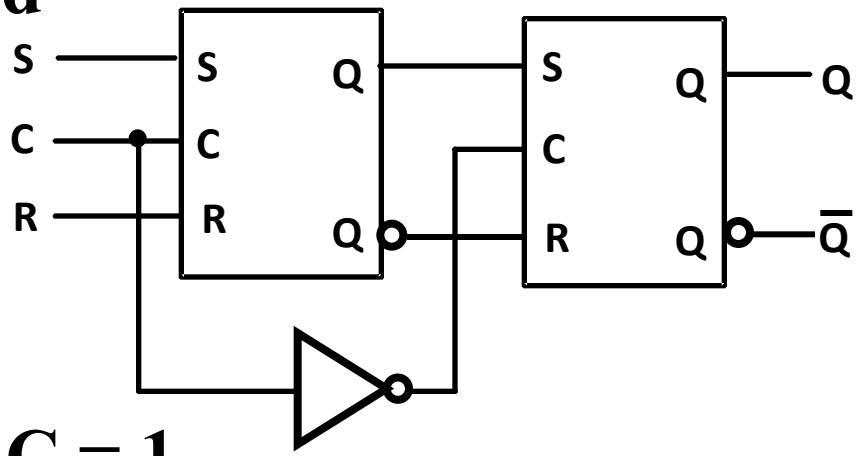
Problems with D-Latch

- If D changes while C is true, the new value of D will appear at the output. The latch is *transparent*.
- If the stored value can change state more than once during a single clock pulse, the result is a hazard that might introduce a glitch later in the circuit.
- We must design the circuit so that the state can change only once per clock cycle.

S-R Master-Slave Flip-Flop

- Consists of two clocked S-R latches in series with the clock on the second latch inverted



- The input is observed by the first latch with C = 1
- The output is changed by the second latch with C = 0
- The path from input to output is broken by the difference in clocking values (C = 1 and C = 0).

Flip-Flop Problem

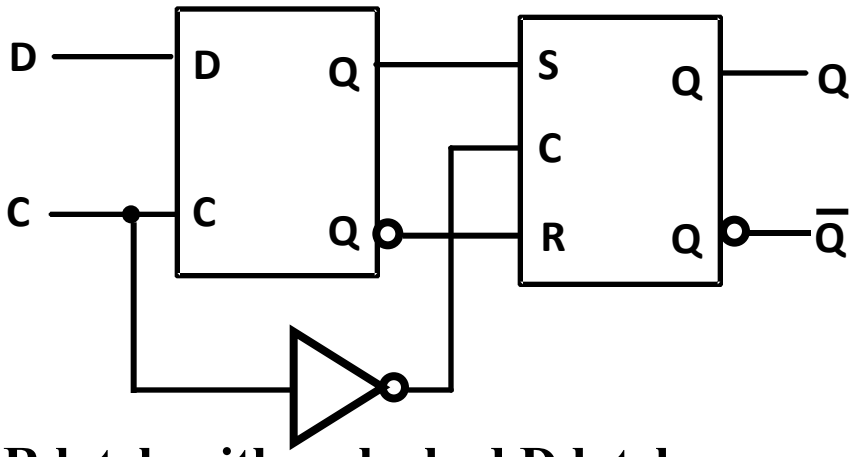
- The change in the flip-flop output is delayed by the pulse width which makes the circuit slower or
- S and/or R are permitted to change while C = 1
  - Suppose Q = 0 and S goes to 1 and then back to 0 with R remaining at 0
    - The master latch sets to 1
    - A 1 is transferred to the slave
  - Suppose Q = 0 and S goes to 1 and back to 0 and R goes to 1 and back to 0
    - The master latch sets and then resets
    - A 0 is transferred to the slave
  - This behavior is called *1s or 0s catching*

Flip-Flop Solution

- Use edge-triggering instead of master-slave
- An *edge-triggered* flip-flop ignores the pulse while it is at a constant level and triggers only during a transition of the clock signal
- Edge-triggered flip-flops can be built directly at the electronic circuit level, or
- A master-slave D flip-flop which also exhibits edge-triggered behavior can be used.

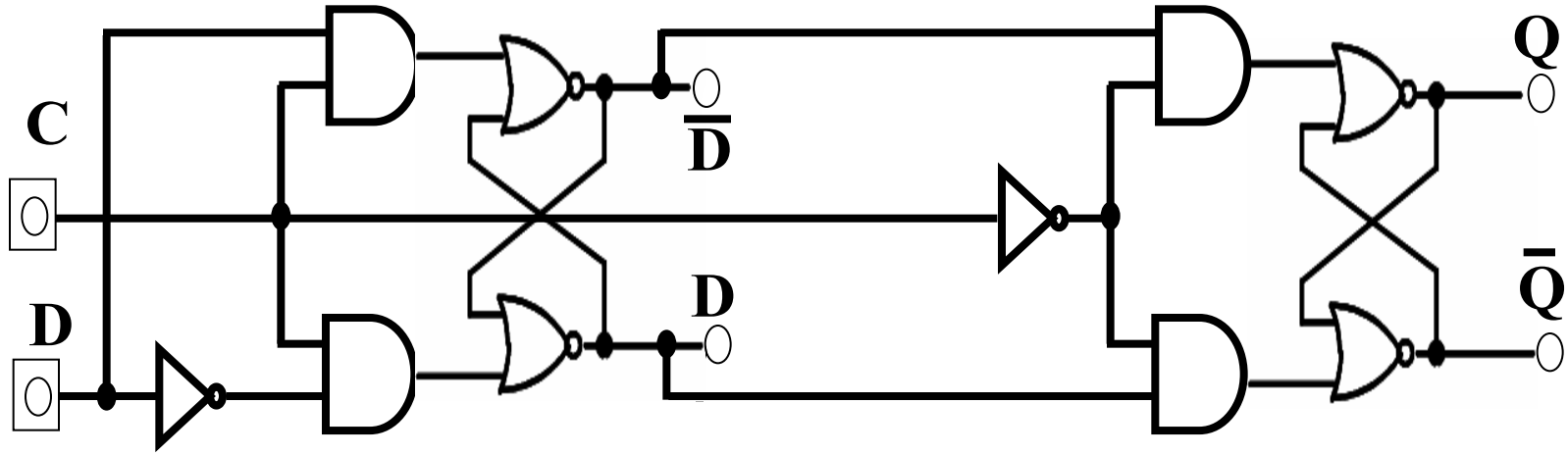
Edge-Triggered D Flip-Flop

- The edge-triggered D flip-flop is the same as the master-slave D flip-flop



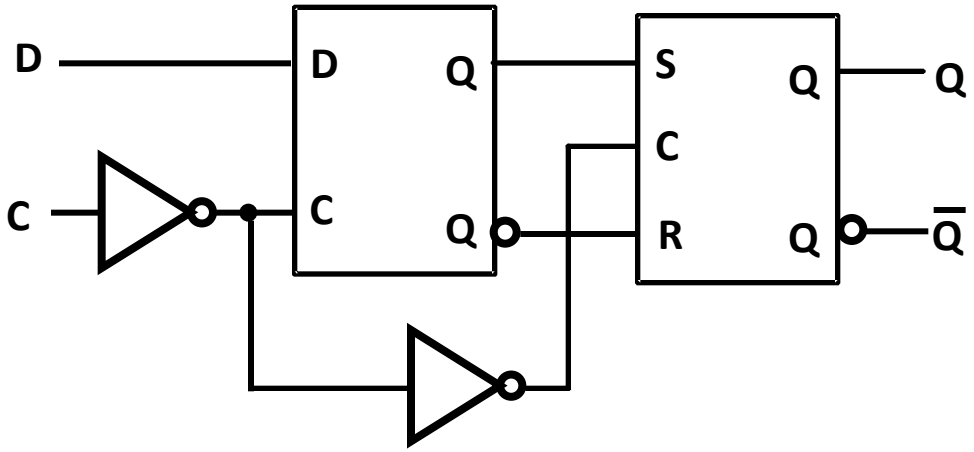
- It can be formed by:
  - Replacing the first clocked S-R latch with a clocked D latch or
  - Adding a D input and inverter to a master-slave S-R flip-flop
- The delay of the S-R master-slave flip-flop can be avoided since the 1s-catching behavior is not present with D replacing S and R inputs
- The change of the D flip-flop output is associated with the negative edge at the end of the pulse
- It is called a *negative-edge triggered* flip-flop

Negative Edge-Triggered D Flip-Flops



Positive-Edge Triggered D Flip-Flop

- Formed by adding inverter to clock input

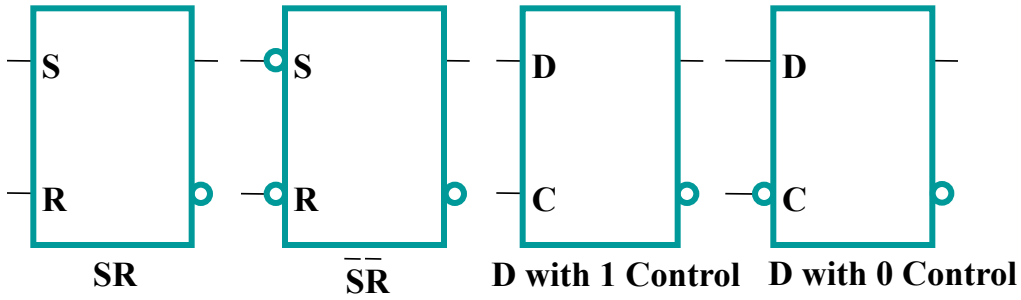


- Q changes to the value on D applied at the positive clock edge within timing constraints to be specified
- Our choice as the standard flip-flop for most sequential circuits

Difference between a LATCH and a FLIP-FLOP ?

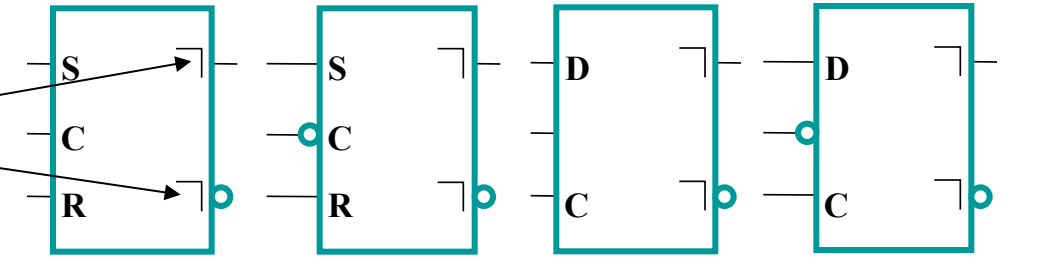
- Latch is a level sensitive device while flip-flop is an edge sensitive device.
- Latch is sensitive to glitches on enable pin, whereas flip-flop is immune to glitches.
- Latches take less gates (also less power) to implement than flip-flops.
- Latches are faster than flip-flops.

Standard Symbols for Storage Elements



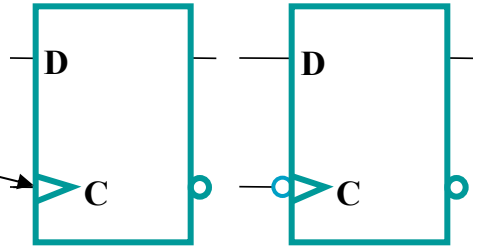
(a) Latches

- **Master-Slave: Postponed output indicators**



(b) Master-Slave Flip-Flops

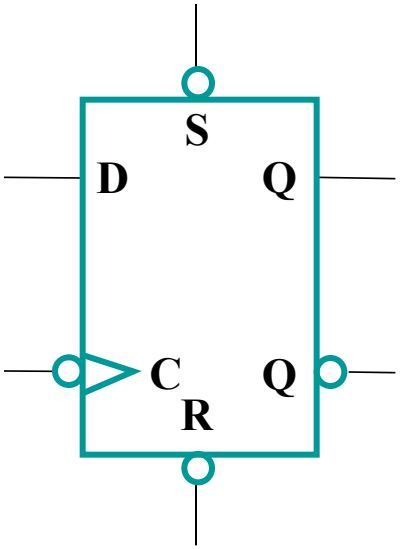
- **Edge-Triggered: Dynamic indicator**



(c) Edge-Triggered Flip-Flops

Direct Inputs

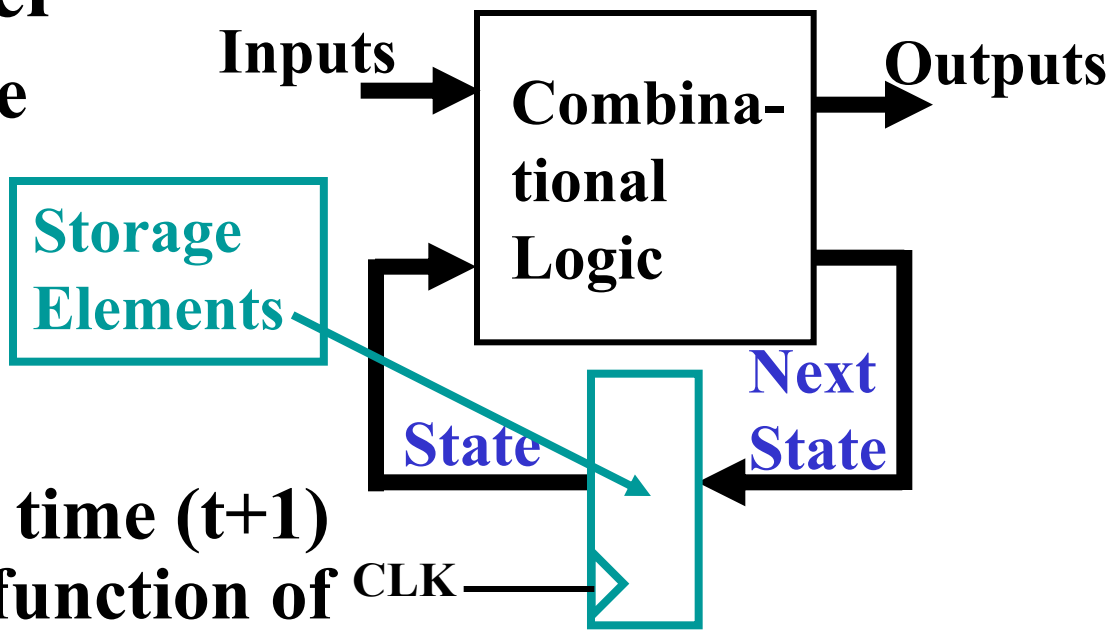
- At power up or at reset, all or part of a sequential circuit usually is initialized to a known state before it begins operation
- This initialization is often done outside of the clocked behavior of the circuit, i.e., asynchronously.



- Direct R and/or S inputs that control the state of the latches within the flip-flops are used for this initialization.
- For the example flip-flop shown
  - 0 applied to $\overline{R}$ resets the flip-flop to the 0 state
  - 0 applied to $\overline{S}$ sets the flip-flop to the 1 state

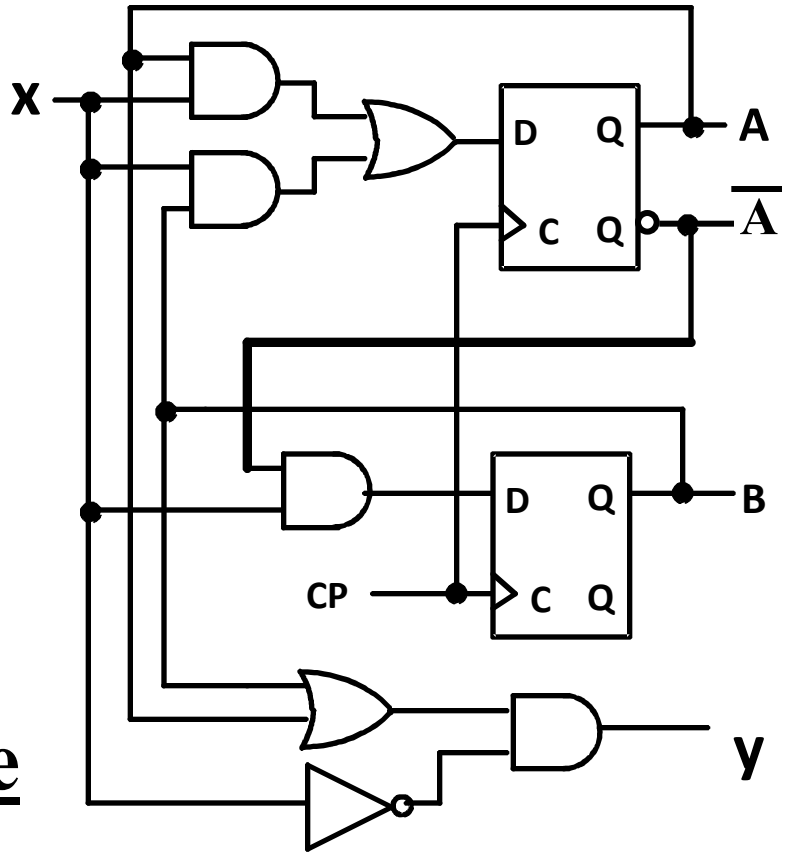
Sequential Circuit Analysis

- **General Model**
  - **Current State at time (t) is stored in an array of flip-flops.**
  - **Next State at time (t+1) is a Boolean function of State and Inputs.**
  - **Outputs at time (t) are a Boolean function of State (t) and (sometimes) Inputs (t).**



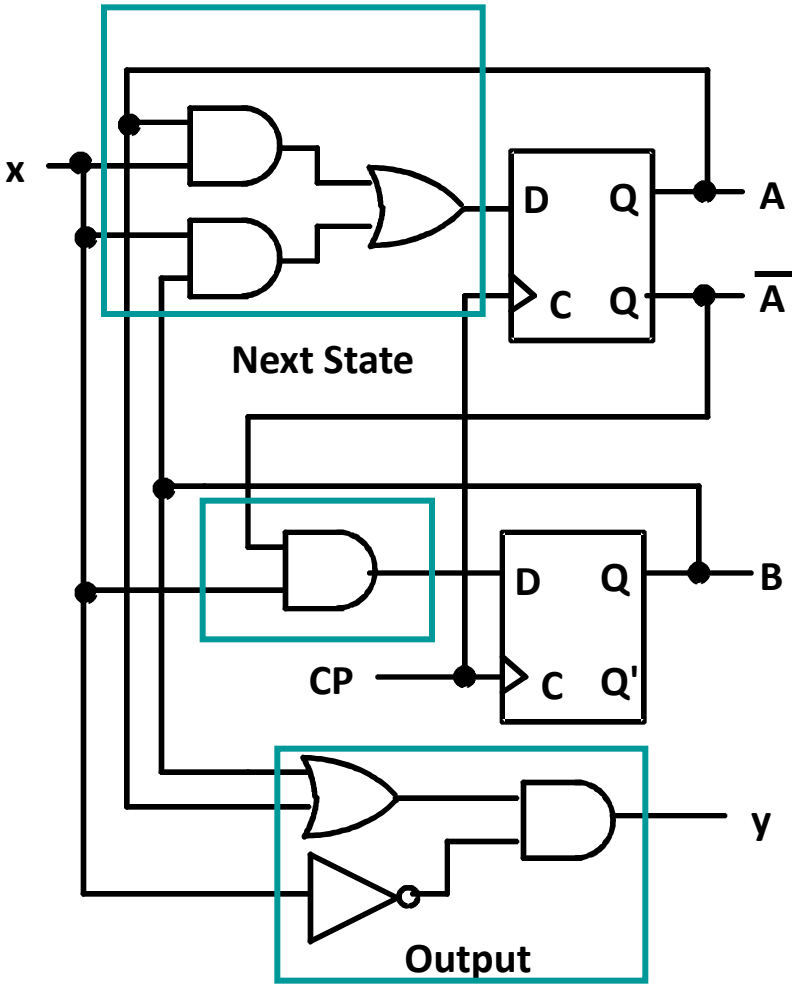
Example 1 (from Fig. 5-15)

- **Input:** x(t)
- **Output:** y(t)
- **State:** (A(t), B(t))
- **What is the Output Function?**
- **What is the Next State Function?**



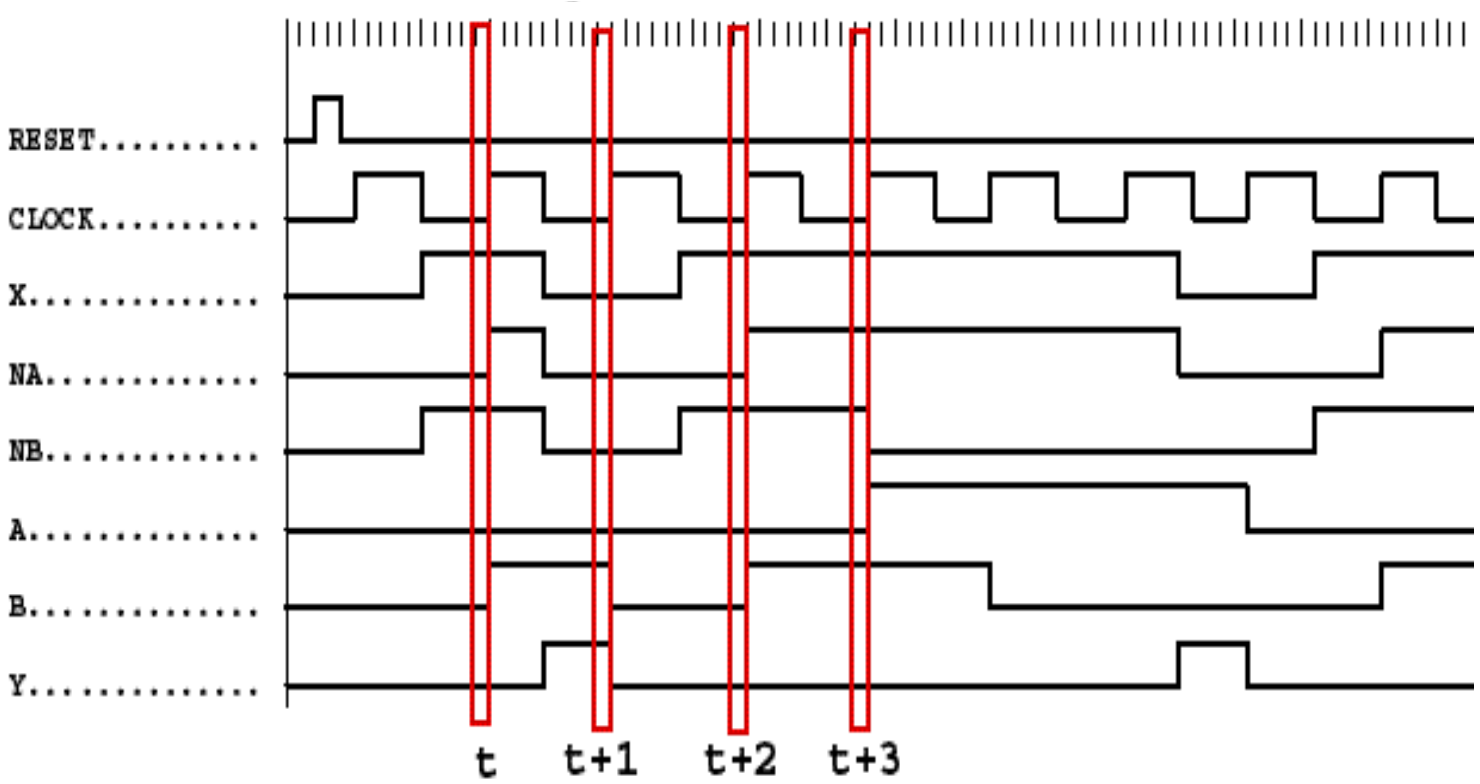
Example 1 (from Fig. 5-15) (continued)

- **Boolean equations for the functions:**
  - $A(t+1) = A(t)x(t) + B(t)x(t)$
  - $B(t+1) = \bar{A}(t)x(t)$
  - $y(t) = \bar{x}(t)(B(t) + A(t))$



Example 1(from Fig. 5-15) (continued)

- **Where in time are inputs, outputs and states defined?**



State Table Characteristics

- ***State table*** **– a multiple variable table with the following four sections:**
  - ***Present State*** **– the values of the state variables for each allowed state.**
  - ***Input*** **– the input combinations allowed.**
  - ***Next-state*** **– the value of the state at time (t+1) based on the present state and the input.**
  - ***Output*** **– the value of the output as a function of the present state and (sometimes) the input.**
- **From the viewpoint of a truth table:**
  - **the inputs are Input, Present State**
  - **and the outputs are Output, Next State**

Example 1: State Table (from Fig. 5-15)

- The state table can be filled in using the next state and output equations: $A(t+1) = A(t)x(t) + B(t)x(t)$
- $B(t+1) = \bar{A}(t)x(t)$
  $y(t) = \bar{x}(t)(B(t) + A(t))$

Present State		Input	Next State		Output
A(t)	B(t)	x(t)	A(t+1)	B(t+1)	y(t)
0	0	0	0	0	0
0	0	1	0	1	0
0	1	0	0	0	1
0	1	1	1	1	0
1	0	0	0	0	1
1	0	1	1	0	0
1	1	0	0	0	1
1	1	1	1	0	0

Example 1: Alternate State Table

- **2-dimensional table that matches well to a K-map.**
  - $A(t+1) = A(t)x(t) + B(t)x(t)$
  - $B(t+1) = \bar{A}(t)x(t)$
  - $y(t) = \bar{x}(t)(B(t) + A(t))$

Present State A(t) B(t)	Next State x(t)=0 A(t+1)B(t+1)	Next State x(t)=1 A(t+1)B(t+1)	Output x(t)=0 y(t)	Output x(t)=1 y(t)
0 0	0 0	0 1	0	0
0 1	0 0	1 1	1	0
1 0	0 0	1 0	1	0
1 1	0 0	1 0	1	0

State Diagrams

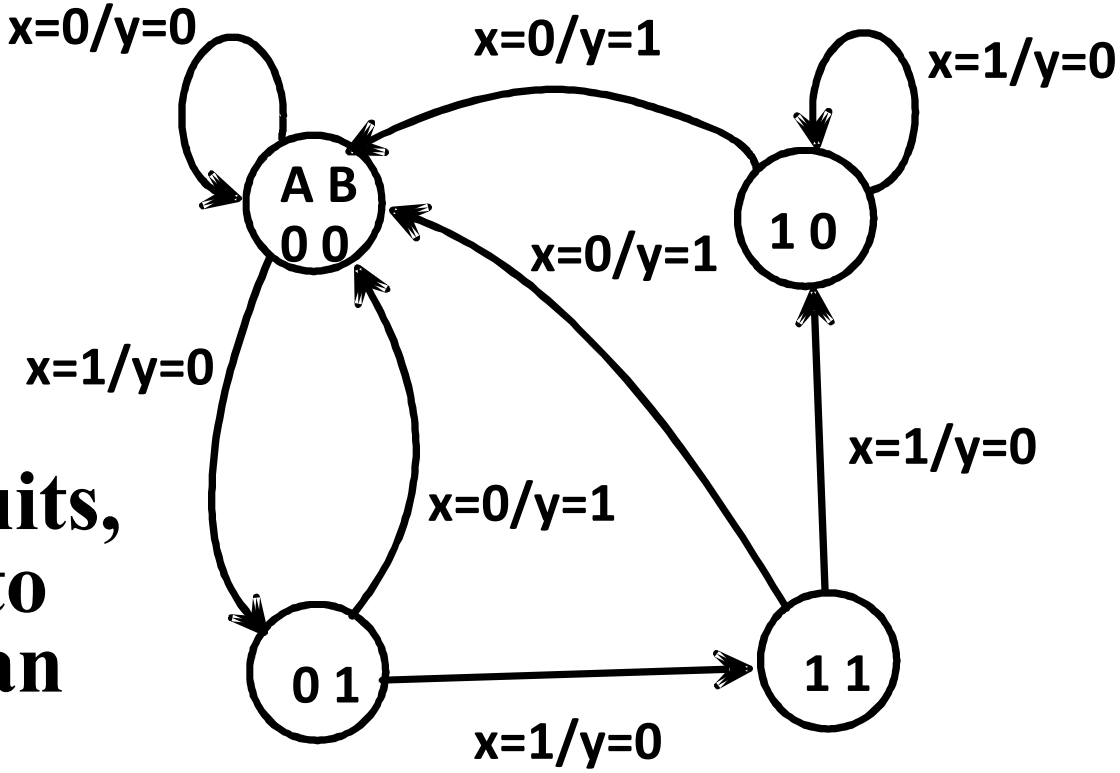
- **The sequential circuit function can be represented in graphical form as a state diagram with the following components:**
  - **A circle with the state name in it for each state**
  - **A directed arc from the Present State to the Next State for each state transition**
  - **A label on each directed arc with the Input values which causes the state transition, and**
  - **A label:**
    - **On each circle with the output value produced, or**
    - **On each directed arc with the output value produced.**

State Diagrams

- **Label form:**
  - **On circle with output included:**
    - **state/output**
    - **Moore type output depends only on state**
  - **On directed arc with the output included:**
    - **input/output**
    - **Mealy type output depends on state and input**

Example 1: State Diagram

- Which type?
- Diagram gets confusing for large circuits
- For small circuits, usually easier to understand than the state table



Moore and Mealy Models

- **Sequential Circuits or Sequential Machines are also called *Finite State Machines* (FSMs). Two formal models exist:**

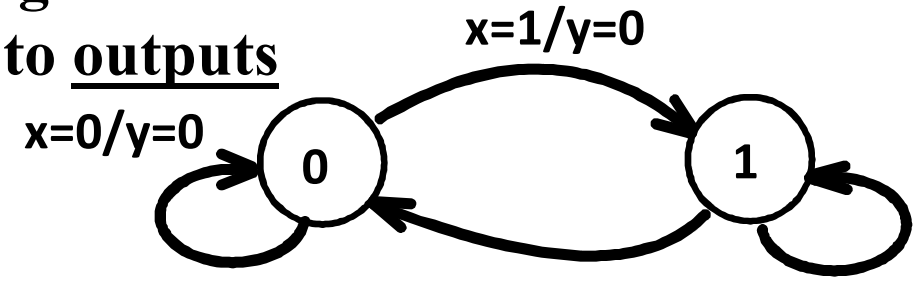
- **Moore Model**
  - **Named after E.F. Moore.**
  - **Outputs are a function ONLY of states**
  - **Usually specified on the states.**

- **Mealy Model**
  - **Named after G. Mealy**
  - **Outputs are a function of inputs AND states**
  - **Usually specified on the state transition arcs.**

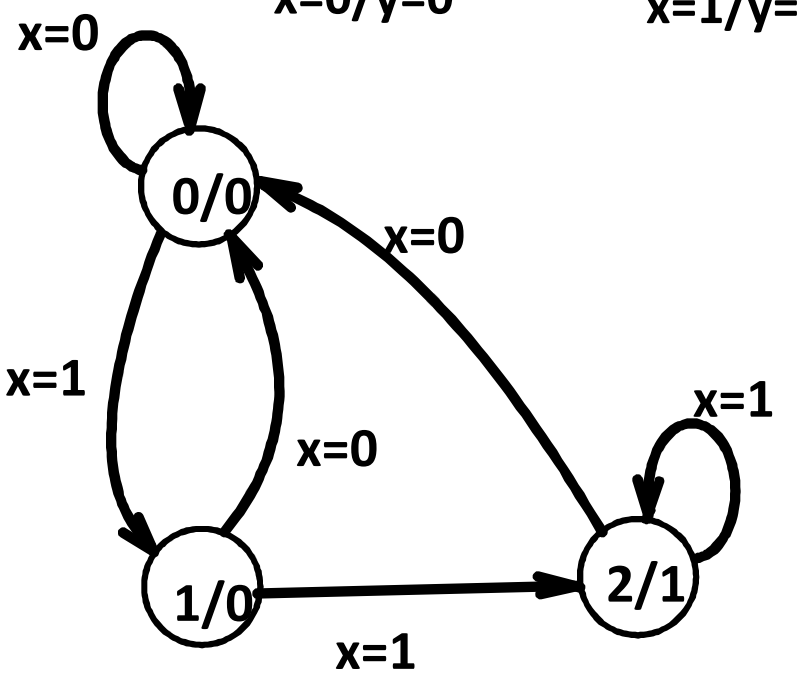
- **In contemporary design, models are sometimes mixed Moore and Mealy**

Moore and Mealy Example Diagrams

- **Mealy Model State Diagram maps inputs and state to outputs**



- **Moore Model State Diagram maps states to outputs**



Moore and Mealy Example Tables

- **Mealy Model state table maps inputs and state to outputs**

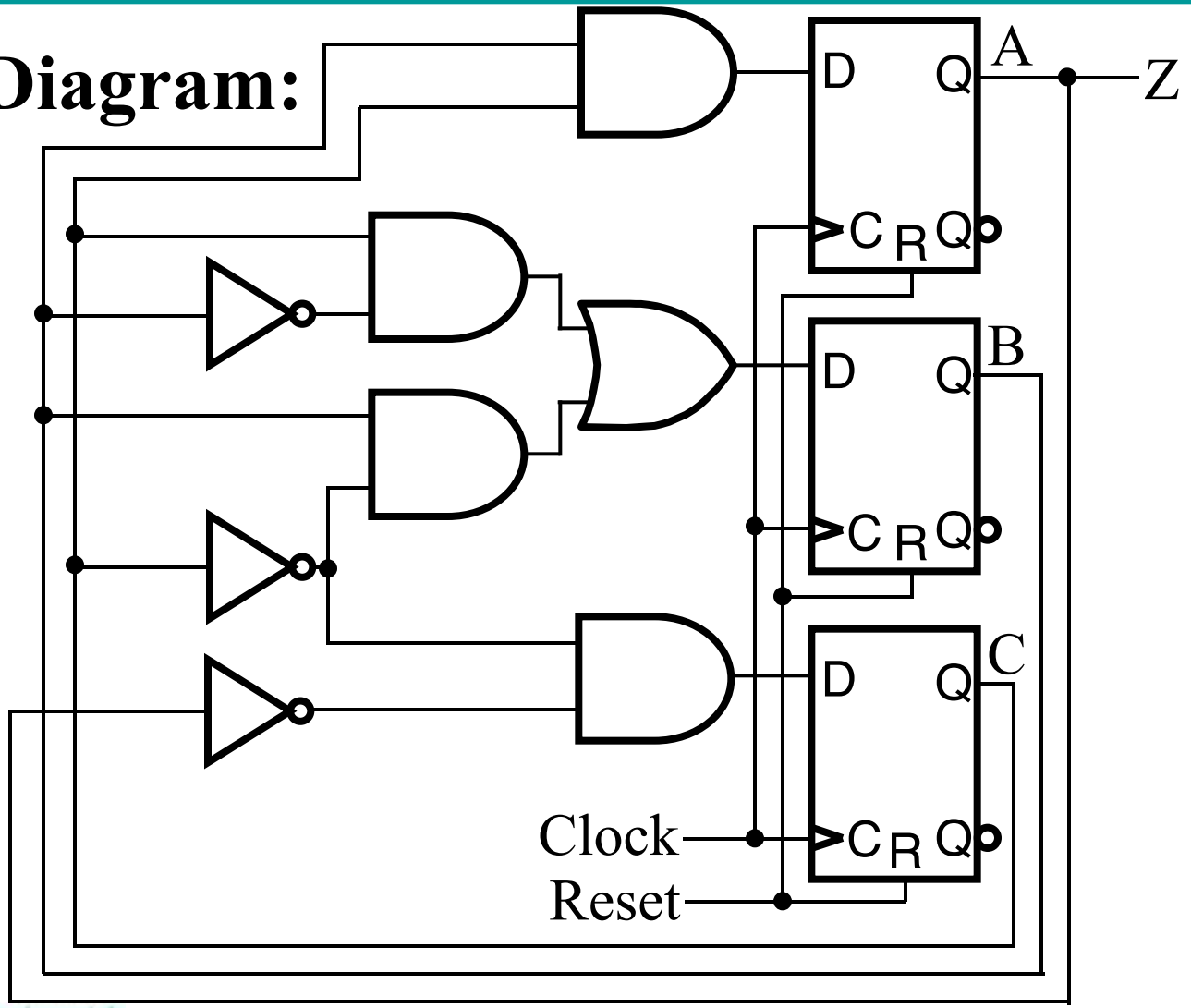
Present State	Next State x=0	Next State x=1	Output x=0	Output x=1
0	0	1	0	0
1	0	1	0	1

- **Moore Model state table maps state to outputs**

Present State	Next State x=0	Next State x=1	Output
0	0	1	0
1	0	2	0
2	0	2	1

Example 2: Sequential Circuit Analysis

- **Logic Diagram:**



Example 2: Flip-Flop Input Equations

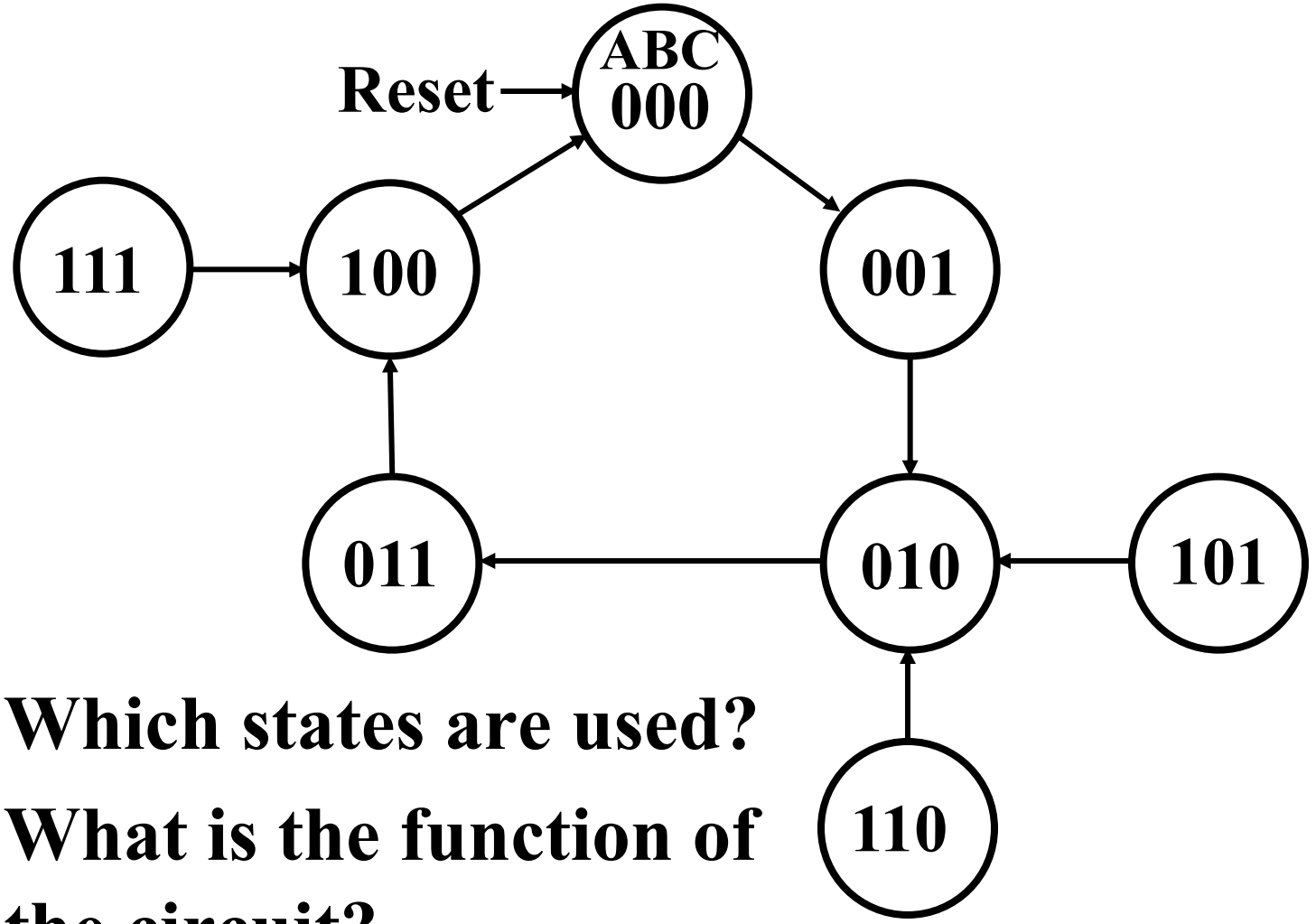
- **Variables**
  - **Inputs: None**
  - **Outputs: Z**
  - **State Variables: A, B, C**
- **Initialization: Reset to (0,0,0)**
- **Equations**
  - **A(t+1) =** **Z =**
  - **B(t+1) =**
  - **C(t+1) =**

Example 2: State Table

$X' = X(t+1)$

A B C	A'B'C'	Z
0 0 0		
0 0 1		
0 1 0		
0 1 1		
1 0 0		
1 0 1		
1 1 0		
1 1 1		

Example 2: State Diagram



- Which states are used?
- What is the function of the circuit?

Weekly Exercises

- 4-5
- 4-8
- 4-9
- 4-10

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- Return to Title Page