Preview for Midterm Exam One Chapter 1

- **Conversion between decimal, binary, and or hexadecimal numbers (including fractions)**

- **Arithmetic operations (addition, subtraction, and multiplication for binary and hexadecimal numbers)**

Chapter 2

- Section 2-2 Boolean Algebra
- Section 2-3 Standard Forms (minterms, SOP)
- Section 2-4 Two-Level Optimization
- Section 2-5 Map Manipulation (PI, EPI, Don’t-Care Conditions)
- Calculate literal cost (L), gate input cost (G and GN)

Chapter 3

- NAND Gate Mapping
- Rudimentary Logic Functions
- Decoder
- Encoder
- Multiplexier and DeMultiplexier
- Design a combinational circuit

Sample Question1

- **Convert decimal number 369.3125 to binary**

- **101110001.0101**

Sample Question2

- **Convert binary number 10111101.101 to decimal**

- **189.625**

Sample Question3

- **Convert hexadecimal number F3C7.A to binary**

- **1111001111000111.101**

Sample Question4

- **Convert binary number 10111101.101 to hexadecimal**

- **BD.A**

Sample Question5

- **Perform following binary multiplication**
- **100111*011011**

```
      100111
     ×011011
     -------
      100111
     100111
    000000
   100111
  100111
 000000
 -----------
 10000011101
```

Sample Question6

- **Perform following hexadecimal multiplication**
- $(543)_{16} * (F0A)_{16}$

			5	4	3	
			F	0	A	
		3	4	9	E	
4	E	E	D			
4	F	2	1	9	E	

Chapter 2

- **Section 2-2 Boolean Algebra**
- **Section 2-3 Standard Forms (minterms, SOP)**
- **Section 2-4 Two-Level Optimization**
- **Section 2-5 Map Manipulation (PI, EPI, Don't-Care Conditions)**
- **Calculate literal cost (L), gate input cost (G and GN)**

Sample Question7

- **Prove the identity of each of the following Boolean equations, using algebraic manipulation**

- **Y + X'Z + XY' = X + Y + Z**

$$Y + \overline{X}Z + X\overline{Y}$$
$$= Y + X\overline{Y} + \overline{X}Z$$
$$= (Y + X)(Y + \overline{Y}) + \overline{X}Z$$
$$= Y + X + \overline{X}Z$$
$$= Y + (X + \overline{X})(X + Z)$$
$$= X + Y + Z$$

Sample Question8

- **Reduce the following Boolean expressions to the indicated number of literals**

- **X'Y' + XYZ + X'Y to three literals**

$$\bar{X}\bar{Y} + XYZ + \bar{X}Y = \bar{X} + XYZ = (\bar{X} + XY)(\bar{X} + Z) = (\bar{X} + X)(\bar{X} + Y)(\bar{X} + Z)$$

$$= (\bar{X} + Y)(\bar{X} + Z) = \bar{X} + YZ$$

Sample Question9

- **Final all the prime implicants for following Boolean functions and determine which are essential.**

- **$F(A,B,C,D)=\sum_m (1, 3, 4, 5, 9, 10, 11, 12, 13, 14, 15)$**

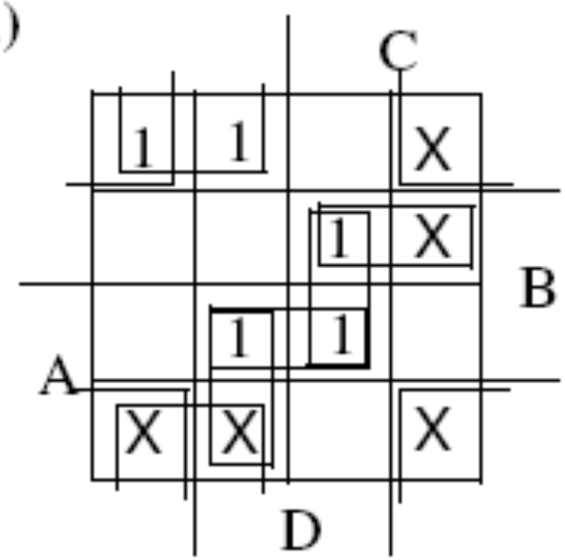
$$Prime = AB, AC, AD, B\overline{C}, \overline{B}D, \overline{C}D$$

$$Essential = AC, B\overline{C}, \overline{B}D$$

Sample Question10

- **Optimize the following Boolean functions F together with the don't-care conditions *d*.**
- **$F(A,B,C,D)= \sum_m (0, 1, 7, 13, 15)$, $d(A,B,C,D)= \sum_m (2, 6, 8, 9, 10)$**

a)



$$F = \overline{B}\,\overline{C} + BCD + ABD$$

Chapter 3

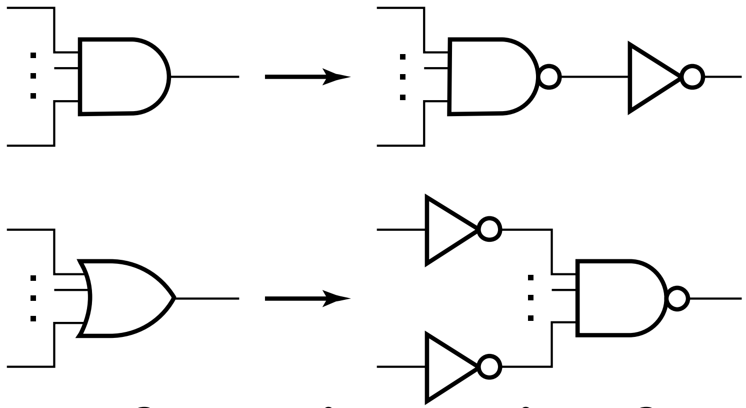
- **NAND Gate Mapping**
- **Rudimentary Logic Functions**
- **Decoder**
- **Encoder**
- **Multiplexier and DeMultiplexier**
- **Design a combinational circuit**

Mapping to NAND gates

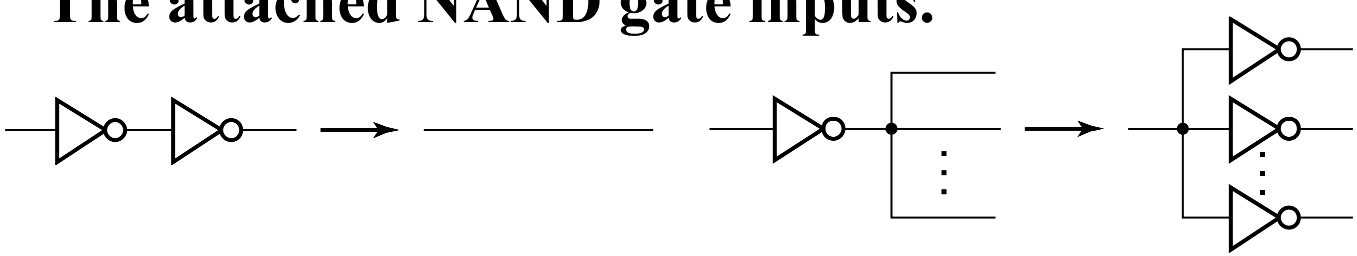
- **Assumptions:**
  - **Gate loading and delay are ignored**
  - **Cell library contains an inverter and *n*-input NAND gates, *n* = 2, 3, …**
  - **An AND, OR, inverter schematic for the circuit is available**
- **The mapping is accomplished by:**
  - **Replacing AND and OR symbols,**
  - **Pushing inverters through circuit fan-out points, and**
  - **Canceling inverter pairs**

NAND Mapping Algorithm

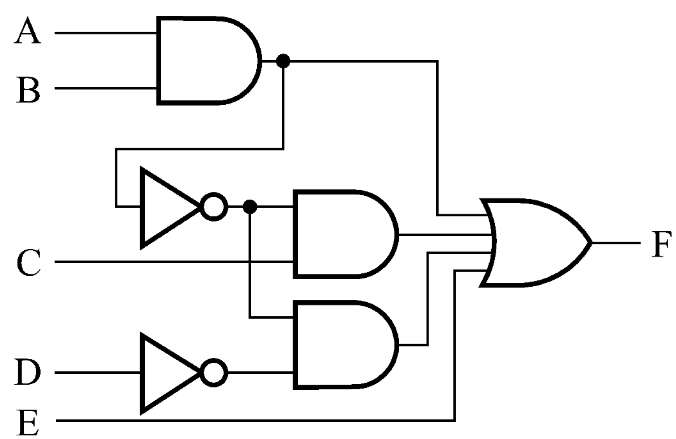
1. Replace ANDs and ORs:



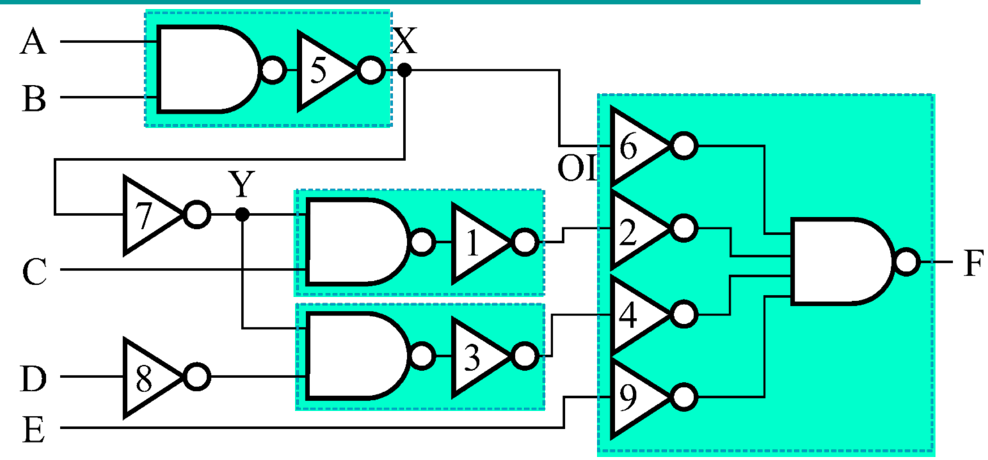
2. Repeat the following pair of actions until there is at most one inverter between :
   a. A circuit input or driving NAND gate output, and
   b. The attached NAND gate inputs.



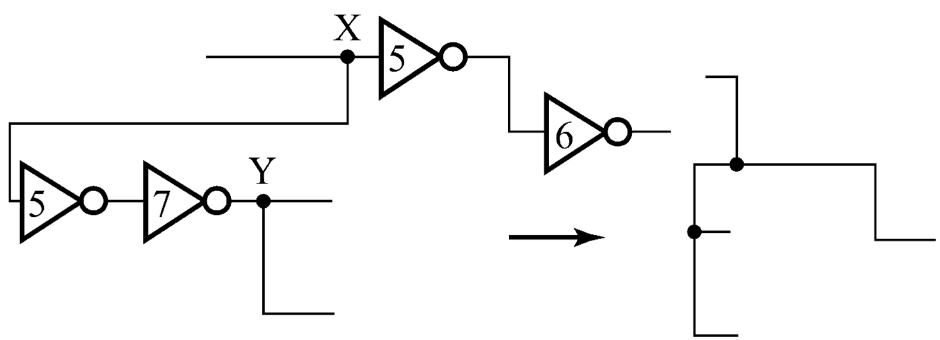
NAND Mapping Example



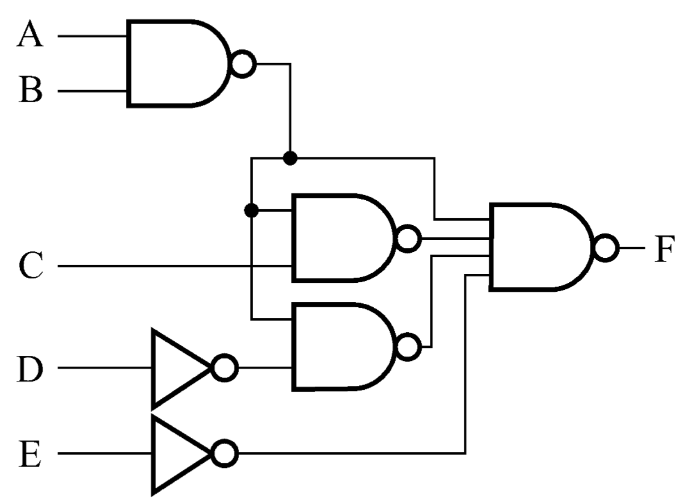
(a)



(b)



(c)



(d)

Sample Question11

- **Q 3-11 (Page 185)**

a)

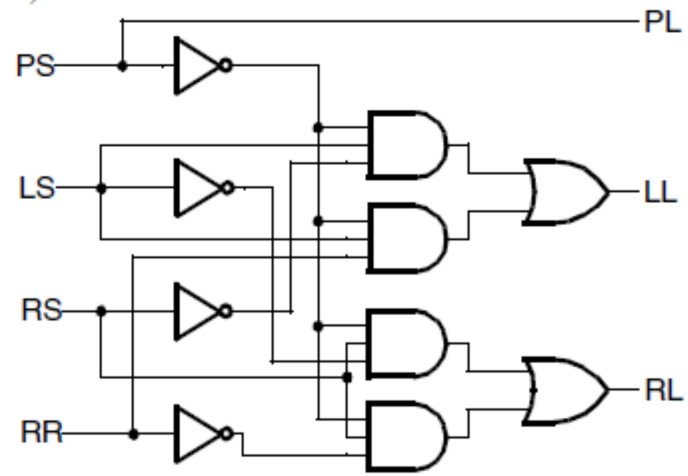
PS	LS	RS	RR	PL	LL	RL
0	0	0	0	0	0	0
0	0	0	1	0	0	0
0	0	1	0	0	0	1
0	0	1	1	0	0	1
0	1	0	0	0	1	0
0	1	0	1	0	1	0
0	1	1	0	0	0	1
0	1	1	1	0	1	0
1	0	0	0	1	0	0
1	0	0	1	1	0	0
1	0	1	0	1	0	0
1	0	1	1	1	0	0
1	1	0	0	1	0	0
1	1	0	1	1	0	0
1	1	1	0	1	0	0
1	1	1	1	1	0	0

$$PL = PS$$

$$LL = \overline{PS}\ LS\ \overline{RS} + \overline{PS}\ LS\ RR$$

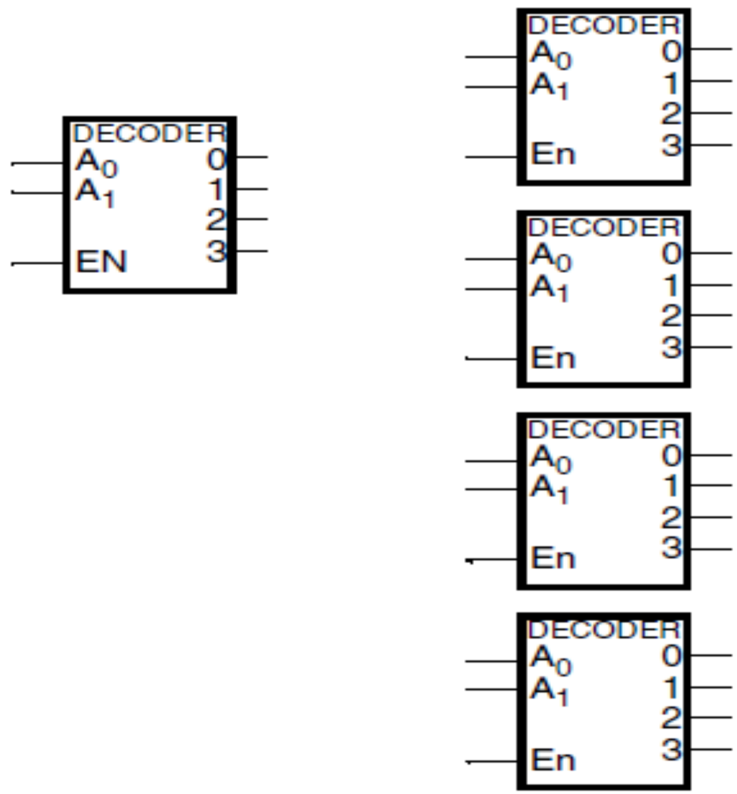
$$RL = \overline{PS}\ \overline{LS}\ RS + \overline{PS}\ RS\ \overline{RR}$$

b)

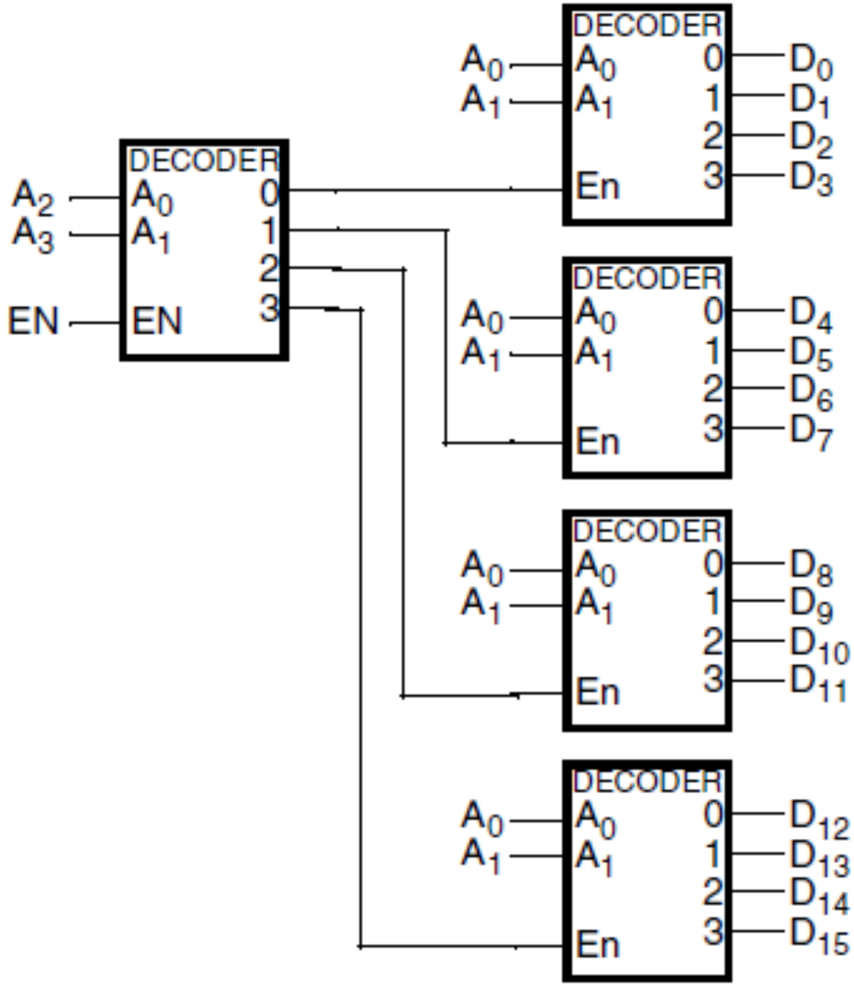


Sample Question12

Design a 4-to-16-line decoder with enable using five 2-to-4-line decoders with enable.



Answer



DECODER
A2
A3
EN
A0
A1
EN
0
1
2
3
DECODER
A0
A1
En
0
1
2
3
D0
D1
D2
D3
DECODER
A0
A1
En
D4
D5
D6
D7
DECODER
A0
A1
En
D8
D9
D10
D11
DECODER
A0
A1
En
D12
D13
D14
D15

Sample Question13

Design a circuit that has a 3-bit binary input and a single output (F) specified as follows:

- **F = 0, when the input is less than $(5)_{10}$**
- **F = 1, otherwise**

Step 1 (Specification):

Label the inputs (3 bits) as X, Y, Z

- X is the most significant bit, Z is the least significant bit

The output (1 bit) is F:

- F = 1 → $(101)_2$, $(110)_2$, $(111)_2$
- F = 0 → other inputs

Sample Question13 (cont.)

Step 2 (Formulation)

Obtain Truth table

X	Y	Z	F
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	0
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1

Boolean Expression:

$F = XY'Z + XYZ' + XYZ$

Step 3 (Optimization)

$F = XY'Z + XYZ' + XYZ$

$= XZ + XY$

Circuit Diagram