San Diego State University

CS 370 Computer Architecture

Homework Assignment #2

- Please type the solutions using a word processor such as WORD, Latex, etc., or write by hand very neatly and legibly, comparable to typing*.
- Please pay special attention to the due date – no late turn ins or special case consideration.
- Please do not email your homework. Instead, please turn in a paper version of your homework in the classroom. Neither the instructor nor the grader will print your homework for you.
- Please do the following problems from the textbook, and submit solutions:

1. Problem 3-28 (**hint:** You can fully use one 3-8 decoder so that you can have 3 inputs and 8 outputs. Meanwhile, you can partially use the second 3-8 decoder so that you have 1 input and 2 outputs. For this second 3-8 decoder, you only need to use one of its inputs [you can connect the other two inputs to the ground so that these two inputs are always zero] and two of its 8 outputs [the other six outputs are simply not used]. Note that each of the two outputs of the second 3-8 decoder controls 8 2-input AND gates)
2. Problem 3-29
3. Probelm 3-36
4. Problem 3-37 (a) (**hint:** An 8x2 AND-OR means 8 AND gates [each of these 8 AND gates has two inputs] and one OR gate with 8 inputs. The 8 outputs of the 8 AND gates are the inputs of the OR gate)
5. Problem 3-52
6. Problem 3-53
7. Problem 3-55
8. Problem 3-57
9. Problem 4-6
10. Problem 4-7
11 . Problem 4-12 (a)
12. Problem 4-17

* The preferred format is typing with a word processor for the following reasons:
1. You have a copy in your computer that you can study for exams or future use.
2. You will learn to use a word processor (if not already learned) to do math, diagrams, etc. This will be one of the most useful things in your career.
3. You have a backup copy in case of lost or misplaced assignment.
4. A typed assignment helps the grader to spend less time and to be more accurate in grading. Our class is multi-national, and it is hard and time consuming to decode many different hand writing styles.

Homework #2 - Tao

3-28. Design a 4–to–16-line decoder using two 3–to–8-line decoders and 16 2-input AND gates.

3-29. Design a 4–to–16-line decoder with enable using five 2–to–4-line decoders with enable as shown in Figure 3-16.

3-36. Derive the truth table of a decimal-to-binary priority encoder. There are 10 inputs I_0 through I_9 and outputs A_3 through A_0 and V. Input I_9 has the highest priority.

3-37. (a) Design an 8–to–1-line multiplexer using a 3–to–8-line decoder and an 8×2 AND-OR.

3-52. Perform the indicated subtraction with the following unsigned binary numbers by taking the 2s complement of the subtrahend:

   (a) $11010 - 10001$

   (b) $11110 - 1110$

   (c) $1111110 - 1111110$

   (d) $101001 - 101$

3-53. Repeat Problem 3-52, assuming the numbers are 2s complement signed numbers. Use extension to equalize the length of the operands. Indicate whether overflow occurs during the complement operations for any of the given subtrahends. Indicate whether overflow occurs overall for any of the given subtractions. When an overflow does occur, repeat the operation with the minimum number of bits required to perform the operation without overflow.

3-55. The following binary numbers have a sign in the leftmost position and, if negative, are in 2s complement form. Perform the indicated arithmetic operations and verify the answers.

   (a) $100111 + 111001$

   (b) $001011 + 100110$

   (c) $110001 - 010010$

   (d) $101110 - 110111$

   Indicate whether overflow occurs for each computation.

3-57. Use contraction beginning with a 4-bit adder with carry out to design a 4-bit increment-by-2 circuit with carry out that adds the binary value 0010 to its 4-bit input. The function to be implemented is $S = A + 0010$.

4-6. A sequential circuit with two D flip-flops A and B, two inputs X and Y, and one output Z is specified by the following input equations:

$$D_A = XA + \overline{X}\overline{Y}, \ D_B = XB + \overline{X}A, \ Z = \overline{X}B$$

   (a) Draw the logic diagram of the circuit.

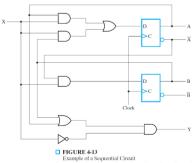   **(b)** Derive the state table.

   (c) Derive the state diagram.

   (d) Is this a Mealy or a Moore machine?

4-7. *A sequential circuit has three D flip-flops A, B, and C, and one input X. The circuit is described by the following input equations:

$$D_A = (B\overline{C} + \overline{B}C)X + (BC + \overline{B}\,\overline{C})\overline{X}$$

$$D_B = A$$

$$D_C = B$$

   (a) Derive the state table for the circuit.

   (b) Draw two state diagrams, one for $X = 0$ and the other for $X = 1$.

4-12. A sequential circuit is given in Figure 4-13.

   (a) Add the necessary logic and/or connections to the circuit to provide an asynchronous reset to state $A = 1$, $B = 0$ for signal $Reset = 0$.

☐ FIGURE 4-13
Example of a Sequential Circuit

4-17. A sequential circuit for a luggage lock has ten pushbuttons labeled 0, 1, 2, 3, 4, 5, 6, 7, 8, and 9. Each pushbutton 0 through 9 produces a 1 on X_i, $i = 0$ through 9, respectively, with all other values on variable X_j, $j \neq i$, equal to 0. Also, these ten pushbuttons produce a positive pulse on the clock C for clocking the flip-flops in the circuit. The circuitry that produces the X_i signals and the clock C has already been designed. The lock opens in response to a sequence of four X_i values, $i = 0, \ldots, 9$, set by the user. The logic for connecting the four selected X_i values to variables X_a, X_b, X_c, and X_d has also been designed. The circuit is locked and reset to its initial state by pushing pushbutton $Lock$, which provides L, the asynchronous reset signal for the circuit. The lock is to unlock in response to the sequence X_a, X_b, X_c, X_d, regardless of all past inputs applied to it since it was reset. The circuit has a single Moore type output U which is 1 to unlock the lock, and 0 otherwise. Design the circuit with inputs X_a, X_b, X_c, and X_d, reset L, clock C, and output U. Use a one-hot code for the state assignment. Implement the circuit with D flip-flops and AND gates, OR gates, and inverters.